Amendments to the Claims:

This listing will replace all prior listing of claims in the application.

Listing of Claims:

1.-3. (Cancelled)

4. (Previously presented) A lateral high-voltage junction device for over voltage protection of an MOS circuit comprising:

a substrate having a first junction region separated from a second junction region by a substrate region;

an MOS gate electrode overlying the substrate region and separated therefrom by a gate oxide layer;

dielectric sidewall spacers adjacent to opposing sides of the MOS gate electrode and overlying the substrate region;

wherein the substrate region is defined by a uniformly doped region of the substrate between the first junction region and second junction region, and

wherein the first junction region comprises an anode and the second junction region comprises a cathode, and wherein the anode and the cathode have an opposite conductivity type.

5. (Previously presented) The device of claim 4, wherein the substrate region separating first and second junction regions has a lateral width of about 200nm or less.

6. (Previously presented) The device of claim 4, wherein the device is configured to support a voltage of greater than about 2.5 volts is across the first and second junction regions.

7. (Previously presented) The device of claim 4, wherein the gate electrode is electrically coupled to the substrate.

8.-10. (Cancelled)

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11. (Previously presented) An input protection circuit comprising:

a voltage supply node and a ground node;

an MOS circuit coupled to the voltage supply node and to the ground node;

a transistor having a first junction region coupled to the voltage supply node, a second junction region coupled to the ground node, and a substrate region between the first and second junction regions,

wherein the transistor functions as a junction diode such that the first junction region comprises a cathode and the second junction region comprises an anode,

wherein the substrate region comprises a junction-free semiconductor region between the first and second junction regions, and

wherein the anode and the substrate region comprise a semiconductor material of the same conductivity type;

an MOS gate electrode overlying the substrate region and separated therefrom by a gate oxide layer; and

dielectric sidewall spacers adjacent to opposing sides of the MOS gate electrode and overlying the substrate region.

12. (Previously presented) The input protection circuit of claim 11 wherein the transistor comprises a plurality of 1 to N forward biased diodes connected in series, such that the first junction region of the first diode is coupled to the voltage supply node and the second junction region of the Nth diode is coupled to the ground node.

13. (Previously presented) The input protection circuit of claim 11 wherein the transistor functions as a lateral bipolar transistor such that the first junction region comprises an emitter and the second junction region comprises a collector.

14. (Cancelled)

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15. (Previously presented) The input protection circuit of claim 11, wherein the source region is coupled to a signal node of an MOS circuit and the drain region is coupled to a ground node of the MOS circuit.

16. (Previously presented) The input protection circuit of ~~claim 15~~ claim 11, wherein a thickness of the gate dielectric layer is substantially the same as a gate dielectric thickness of the MOS circuit.

17. (Cancelled)

18. (Previously presented) The input protection circuit of claim 11, wherein the transistor is configured to support a voltage of greater than about 2.5 volts across the source and drain regions.

19. (Previously presented) The circuit of claim 11, wherein the MOS gate electrode is electrically coupled to the substrate.

20. (Previously presented) The circuit of claim 11, wherein the substrate region is defined by a uniformly doped region between the source region and the drain region.

21. (Cancelled)

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